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PRODUCT BRIEF

LICENSABLE INTELLECTUAL PROPERTY FOR FPGA, ASIC OR ASSP DESIGNS

1G

Ultra-Low Latency 1G Ethernet MAC and PCS

APPLICATIONS

- High Frequency Trading
- Smart NIC
- Low-Latency Switches
- Low-Latency Radio
- Test and Monitoring Equipment

ULTRA-LOW LATENCY, HIGH-SPEED, FLEXIBILITY AND SCALABILITY.

The Ultra-Low Latency 1G Ethernet MAC and PCS is the industry leading solution for latency critical Ethernet applications. The core is designed using advanced design techniques leading to unmatched ultra-low gate count utilization and amazing latency performances.

It includes a rich set of standard and advanced features making it ideal for a large number of applications. The IP core can support full wire line speed with a 64-byte packet length. It also supports back-to-back or mixed length traffic, up to jumbo frame size, with no dropped packets.

GENERAL FEATURES

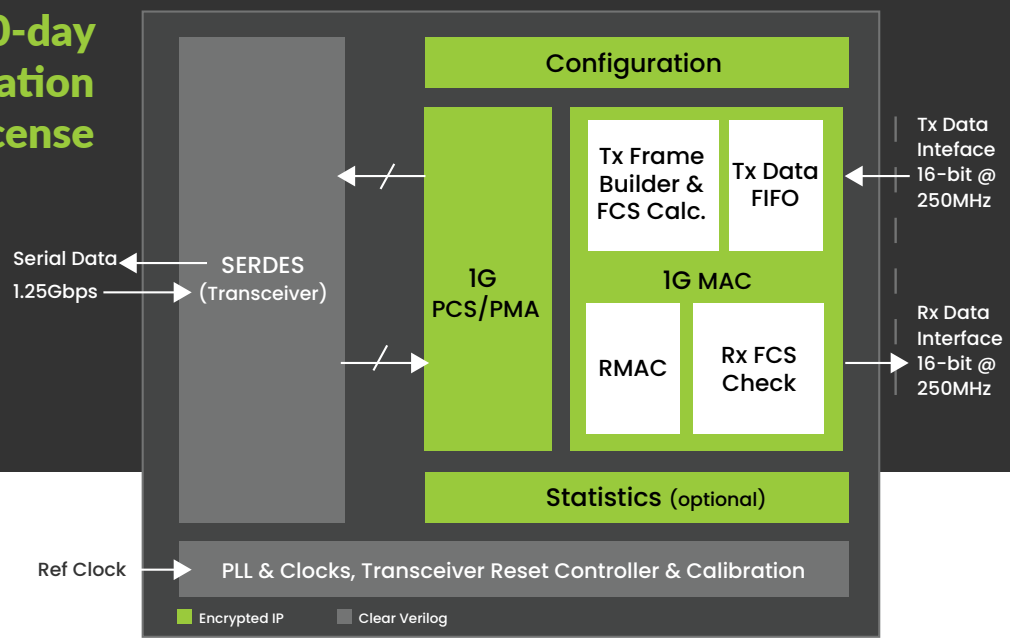
Compliant with the IEEE 802.3-2012 High Speed Ethernet Standard	Ethernet MAC supports 1GbE line rate with flexible feature set	Soft PCS logic interfacing to standard serial transceiver at 1.25Gbps

1G

Ultra-Low Latency 1G Ethernet MAC and PCS

Free 30-day evaluation license

HIGH-LEVEL BLOCK DIAGRAM



DELIVERABLES

- **Datasheet & user guide**
- **Encrypted Verilog**
- **Constraints file**
- **Reference design**
- **Technical support**
- **Optional Verification IP (UVM based)**
- **Optional IP design customization**

MAC FEATURES

- Deficit idle counter (DIC) to maintain a 12-byte inter-packet gap (IPG) average
- Programmable IPG length (down to 1-byte)
- Programmable Maximum Receive Unit (MRU), Maximum Transmission Unit
- User facing logic interface 16-bit @ 250MHz
- Ethernet flow control and congestion management using pause frames with programmable quanta
- Programmable Tx minimum packet length with enable/disable padding option
- Programmable Rx minimum packet length
- Tx Frame Check Sequence (FCS) computation and insertion
- Programmable Tx FCS pass-through and corruption insertion modes
- Programmable keep/strip Rx FCS
- Programmable Rx FCS error detection and marking
- Programmable Tx and Rx path VLAN detection (Programmable TPID, stacked VLAN)
- Configurable statistics vector and collector on transmit and receive MAC data

PCS FEATURES

- Supports 1000BASE-X PHY based on 8B/10B encoding
- Running disparity compute
- Configurable statistics vector and collector on transmit and receive PCS

ORDERING INFORMATION

ENET-001G-L-01 (1G)

sales@orthogone.com
514.316.1917 x703

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PERFORMANCES OVERVIEW EXAMPLE

Device Family (1)	Rate [Gbps]	Resources Utilization (2)			Core clock [MHz]	Wire to Wire Round-Trip Latency (3)
		LUTs	FFs	BRAM		
UltraScale +	1-Gbps	2.28k	4.14k	0	250	136ns

(1) Other FPGA platforms supported (2) Resources utilization includes statistics counters (3) Latency: GTY Transceiver + PCS + MAC (Tx+Rx)

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PRODUCT BRIEF

LICENSABLE INTELLECTUAL PROPERTY FOR FPGA, ASIC OR ASSP DESIGNS

10G

Ultra-Low Latency 10G Ethernet MAC and PCS

ULTRA-LOW LATENCY, HIGH-SPEED, FLEXIBILITY AND SCALABILITY.

APPLICATIONS

- High Frequency Trading
- Smart NIC
- Low-Latency Switches
- QoS-Based Packet Processing
- Test and Monitoring Equipment
- Backhaul Solution

The Ultra-Low Latency 10G Ethernet MAC and PCS is the industry leading solution for latency critical Ethernet applications. The core is designed using advanced design techniques leading to unmatched ultra-low gate count utilization and amazing latency performances. It includes a rich set of standard and advanced features making it ideal for a large number of applications.

The IP core can support full wire line speed with a 64-byte packet length. It also supports back-to-back or mixed length traffic, up to jumbo frame size, with no dropped packets.

GENERAL FEATURES

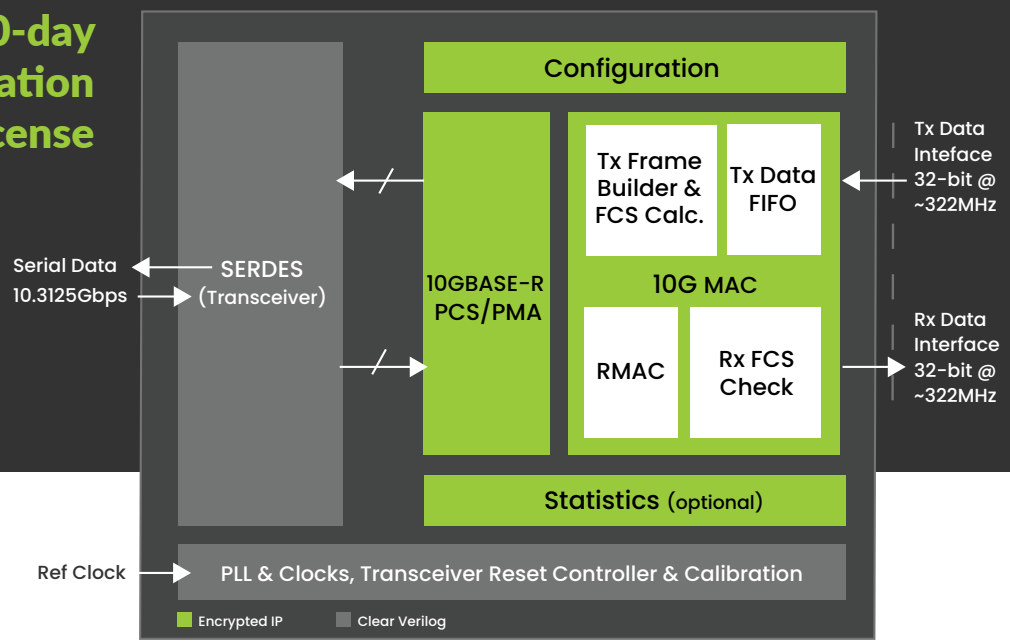
Compliant with the IEEE 802.3-2012 High Speed Ethernet Standard	Ethernet MAC supports 10GbE line rate with flexible feature set	Soft PCS logic interfacing to standard serial transceiver at 10.3125Gbps

10G

Ultra-Low Latency 10G Ethernet MAC and PCS

Free 30-day evaluation license

HIGH-LEVEL BLOCK DIAGRAM



DELIVERABLES

- **Datasheet & user guide**
- **Encrypted Verilog**
- **Constraints file**
- **Reference design**
- **Technical support**
- **Optional Verification IP (UVM based)**
- **Optional IP design customization**

MAC FEATURES

- Deficit idle counter (DIC) to maintain a 12-byte inter-packet gap (IPG) average
- Programmable IPG length (down to 1-byte)
- Programmable Maximum Receive Unit (MRU), Maximum Transmission Unit
- User facing logic interface 32-bit @ 322.265625MHz
- Ethernet flow control and congestion management using pause frames with programmable quanta
- Programmable Tx minimum packet length with enable/disable padding option
- Programmable Rx minimum packet length
- Tx Frame Check Sequence (FCS) computation and insertion
- Programmable Tx FCS pass-through and corruption insertion modes
- Programmable keep/strip Rx FCS
- Programmable Rx FCS error detection and marking
- Programmable Tx and Rx path VLAN detection (Programmable TPID, stacked VLAN)
- Configurable statistics vector and collector on transmit and receive MAC data

PCS FEATURES

- Supports 10GBASE-R PHY based on 64B/66B encoding and scrambling
- Supports block synchronization and BER monitor
- Configurable statistics vector and collector on transmit and receive PCS

ORDERING INFORMATION

ENET-010G-L-01 (10G)

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514.316.1917 x703

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PERFORMANCES OVERVIEW EXAMPLE

Device Family (1)	Rate [Gbps]	Resources Utilization (2)			Core clock [MHz]	Wire to Wire Round-Trip Latency (3)
		LUTs	FFs	BRAM		
UltraScale +	10-Gbps	3.31k	5.16k	0	322.265	67ns

(1) Other FPGA platforms supported: Intel PSG: Stratix-V, Arria-10, Xilinx: Series-7, UltraScale.
(2) Resources utilization includes statistics counters (3) Latency: GTY Transceiver + PCS + MAC (Tx + Rx)

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PRODUCT BRIEF

LICENSABLE INTELLECTUAL PROPERTY FOR FPGA, ASIC OR ASSP DESIGNS

25G

Ethernet MAC and PCS + RS-FEC

APPLICATIONS

- Data Centers
- Smart NIC
- Low-Latency Switches
- QoS-Based Packet Processing
- Test and Monitoring Equipment
- Backhaul Solution
- Video over IP

ULTRA-LOW LATENCY, HIGH-SPEED, FLEXIBILITY AND SCALABILITY.

The 25G Ethernet MAC & PCS + RS-FEC is compliant with IEEE802.3by -2016 and 25/50G Ethernet Consortium specifications. The core is designed using advanced design techniques leading to unmatched ultra-low gate count utilization and great latency performances. It includes a rich set of standard and advanced features making it ideal for a large number of applications.

The IP core can support full wire line speed with a 64-byte packet length. It also supports back-to-back or mixed length traffic, up to jumbo frame size, with no dropped packets.

The core includes Reed Solomon FEC RS(528, 514, 10) with FEC bypass and error correction bypass capabilities. A second option of the IP core without RS-FEC is also available.

GENERAL FEATURES

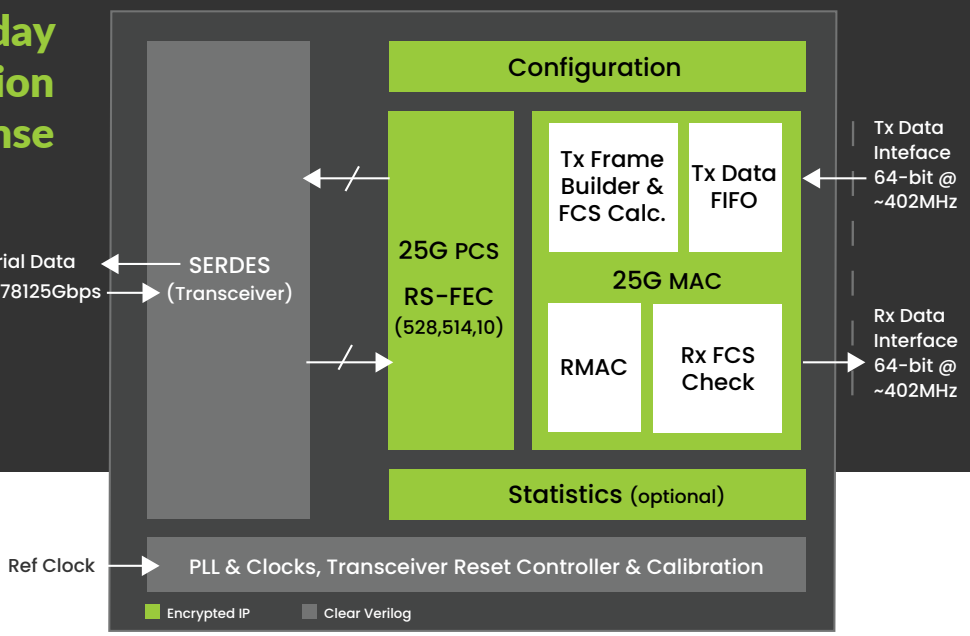
Compliant with IEEE802.3by-2016 and 25/50G Ethernet Consortium	Ethernet MAC supports 25GbE line rate with flexible feature set	Soft PCS logic interfacing to standard serial transceiver at 25.78125Gbps

25G

Ethernet MAC
and PCS + RS-FEC

Free 30-day evaluation license

HIGH-LEVEL BLOCK DIAGRAM



KEY BENEFITS

- **Industry leading performances**
- **Ultra-low gate count**
- **Ultra-low latency**
- **Ease of use**
- **Flexibility & scalability**
- **Supports wide range of FPGA devices**
- **High timing margin**

MAC FEATURES

- Deficit idle counter (DIC) to maintain a 12-byte inter-packet gap (IPG) average
- Programmable IPG length
- Programmable Maximum Receive Unit (MRU), Maximum Transmission Unit
- User facing logic interface 64-bit @ ~402.8MHz
- Ethernet flow control and congestion management using pause frames with programmable quanta
- Programmable Tx minimum packet length with enable/disable padding option
- Programmable Rx minimum packet length
- Tx Frame Check Sequence (FCS) computation and insertion
- Programmable Tx FCS pass-through and corruption insertion modes
- Programmable keep/strip Rx FCS
- Programmable Rx FCS error detection and marking
- Programmable Tx and Rx large frame threshold detection
- Programmable Tx and Rx path VLAN detection (Programmable TPID, stacked VLAN)
- Programmable Rx frame discard & marking
- Configurable statistics vector and collector on transmit and receive MAC data

PCS FEATURES

- Supports 25GBASE-R PHY based on 64B/66B encoding and scrambling
- Supports block synchronization and BER monitor
- Configurable statistics vector and collector on transmit and receive PCS

25G
Ethernet MAC
and PCS + RS-FEC

PRODUCT BRIEF

DELIVERABLES

- Datasheet & user guide
- Encrypted Verilog
- Constraints file
- Reference design
- Technical support
- Optional Verification IP (UVM based)
- Optional IP design customization

ORDERING INFORMATION

25G MAC+PCS
ENET-025G-L-01

25G MAC+PCS + RS-FEC
ENET-025G-R-01

sales@orthogone.com
514.316.1917 x703

RS-FEC FEATURES

- Built-In Reed Solomon FEC RS(528, 514, 10) with FEC bypass and error correction bypass capabilities
- Pre-compilation setting to include or not RS-FEC option (MAC/PCS/PMA or MAC/PCS/PMA + RS-FEC)
- Statistics information for RS-FEC decoder (FEC align status, corrected & uncorrected FEC codewords)

PERFORMANCES OVERVIEW

25G MAC/PCS

Device Family (1)	Rate [Gbps]	Resources Utilization (2)			Core clock [MHz]	Wire to Wire Round-Trip Latency (3)
		LUTs ALMs	FFs	BRAM		
UltraScale +	25-Gbps	4.98k	7.34k	0	~ 402MHz	114 ns
Stratix-10	25-Gbps	4.68k	8.26k	< 1%	~ 402MHz	134 ns

25G MAC/PCS + RS-FEC

Device Family (1)	Rate [Gbps]	Resources Utilization (2)			Core clock [MHz]	Wire to Wire Round-Trip Latency (3)
		LUTs ALMs	FFs	BRAM		
UltraScale +	25-Gbps	13.1k	14.4k	5	~ 402MHz	713 ns
Stratix-10	25-Gbps	12.5k	20.8k	< 1%	~ 402MHz	730 ns

(1) Other FPGA platforms are also supported. Performances provided for mid speed grade (-2).
(2) Resources utilization includes statistics counters
(3) Latency: Transceiver + PCS + MAC (Tx + Rx)

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PRODUCT BRIEF

LICENSABLE INTELLECTUAL PROPERTY FOR FPGA, ASIC OR ASSP DESIGNS

40/100G

Ethernet MAC and PCS + RS-FEC

ULTRA-LOW LATENCY, HIGH-SPEED, FLEXIBILITY AND SCALABILITY.

The 40/100G Ethernet MAC & PCS + RS-FEC is a multi-rate IP core supporting 40G and 100G line rate. The core is designed using advanced design techniques leading to unmatched ultra-low gate count utilization and great latency performances. It includes a rich set of standard and advanced features making it ideal for a large number of applications.

The IP core can support full wire line speed with a 64-byte packet length. It also supports back-to-back or mixed length traffic, up to jumbo frame size, with no dropped packets.

The core includes Reed Solomon FEC RS(528, 514, 10) with FEC bypass and error correction bypass capabilities. Two other versions of the IP core are also available, each supporting a single rate, i.e. 40Gbps or 100Gbps (with RS-FEC).

APPLICATIONS

- Data Centers
- Smart NIC
- Low-Latency Switches
- QoS-Based Packet Processing
- Test and Monitoring Equipment
- Backhaul Solution
- Video over IP

GENERAL FEATURES

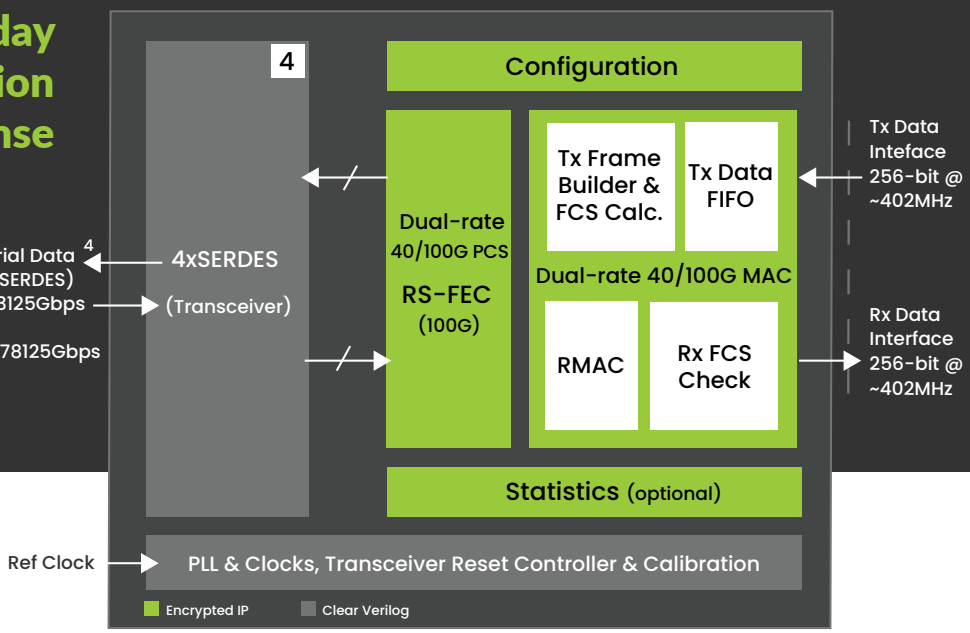
Compliant with IEEE802.3-2015 standard	Ethernet MAC supports 40GbE and 100GbE line rate with flexible feature set	Soft PCS logic interfacing to standard serial transceiver at 10.3125Gbps and 25.78125Gbps

40/100G

Ethernet MAC and PCS + RS-FEC

Free 30-day evaluation license

HIGH-LEVEL BLOCK DIAGRAM



KEY BENEFITS

- **Industry leading performances**
- **Ultra-low gate count**
- **Ultra-low latency**
- **Ease of use**
- **Flexibility & scalability**
- **Supports wide range of FPGA devices**
- **High timing margin**

MAC FEATURES

- Deficit idle counter (DIC) to maintain a 12-byte inter-packet gap (IPG) average
- Programmable IPG length
- Programmable Maximum Receive Unit (MRU), Maximum Transmission Unit
- User facing logic interface 256-bit @ ~402.8MHz
- Ethernet flow control and congestion management using pause frames with programmable quanta
- Programmable Tx minimum packet length with enable/disable padding option
- Programmable Rx minimum packet length
- Tx Frame Check Sequence (FCS) computation and insertion
- Programmable Tx FCS pass-through and corruption insertion modes
- Programmable keep/strip Rx FCS
- Programmable Rx FCS error detection and marking
- Programmable Tx and Rx large frame threshold detection
- Programmable Tx and Rx path VLAN detection (Programmable TPID, stacked VLAN)
- Programmable Rx frame discard & marking
- Configurable statistics vector and collector on transmit and receive MAC data

PCS FEATURES

- Supports 40GBASE-R and 100GBASE-R PHY based on 64B/66B encoding with data striping and alignment markers to align data from multiple lanes
- Supports block synchronization and BER monitor
- Supports multiple lanes swapping, lane alignment and deskew
- Configurable statistics vector and collector on transmit and receive PCS

PRODUCT BRIEF

40/100G

Ethernet MAC and PCS + RS-FEC

DELIVERABLES

- Datasheet & user guide
- Encrypted Verilog
- Constraints file
- Reference design
- Technical support
- Optional Verification IP (UVM based)
- Optional IP design customization

RS-FEC FEATURES

- Built-In Reed Solomon FEC RS(528, 514, 10) with FEC bypass and error correction bypass capabilities
- Statistics information for RS-FEC decoder (FEC align status, corrected & uncorrected FEC codewords)

PERFORMANCES OVERVIEW

MULTI-RATE 40/100G MAC & PCS + RS-FEC

Device Family (1)	Rate [Gbps]	Resources Utilization (2)			Core clock [MHz]	Wire to Wire Round-Trip Latency (3)
		LUTs	FFs	BRAM		
UltraScale +	40-Gbps	44.2k	43.6k	21	~ 402MHz	315 ns
UltraScale +	100-Gbps (RS-FEC Off)					196 ns
UltraScale +	100-Gbps (RS-FEC On)					399 ns

(1) Other FPGA platforms are also supported. Performances provided for mid speed grade (-2).
(2) Resources utilization includes statistics counters
(3) Latency: Transceiver + PCS + MAC (Tx + Rx)
Contact us for the performance of other product variants

ORDERING INFORMATION

ENET-100G-R-02
(40/100G + RS-FEC)

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