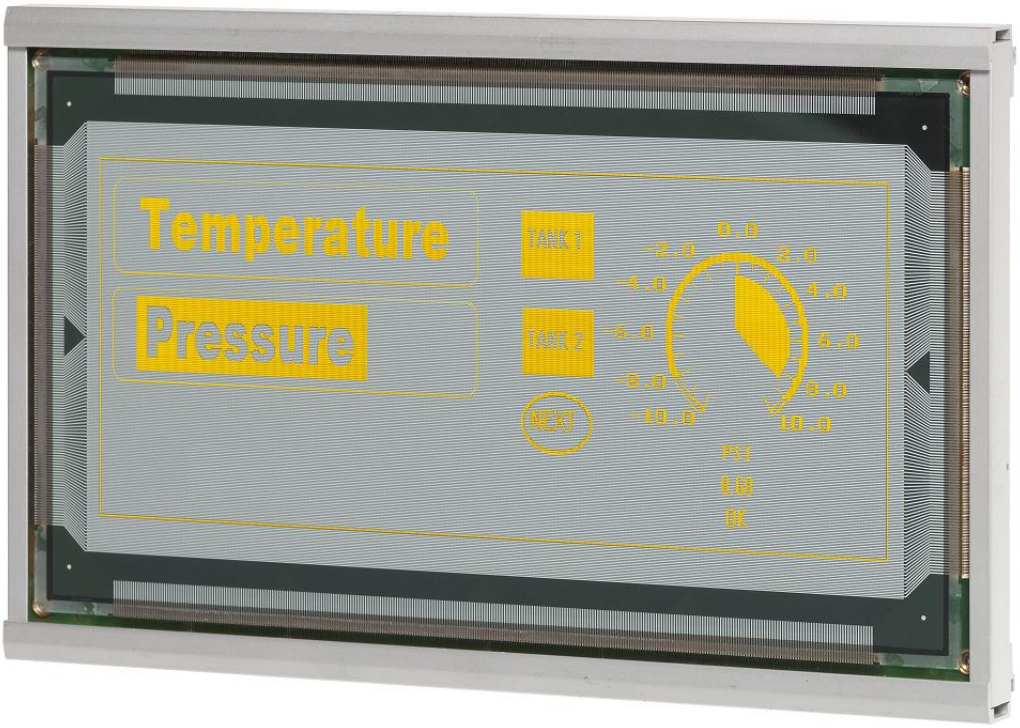

EL512.256-H3 Series (8.6”)

Operation Manual

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1 Product profile

The EL512.256–H3 series displays are rugged, high-resolution thin film electroluminescent (TFEL) flat panel displays. They feature an integrated DC/DC converter, and their compact dimensions save space that allows addition of features or reduction in overall size. They are designed to work in extreme environments and the crisp display is viewable at wide viewing angles both in horizontal and vertical directions. Their ease of installation reduces system integration costs.

The EL512.256–H3 is a 512 column by 256 row flat panel display with a 1:1 pixel aspect ratio. The digital flat panel interface is designed to match the needs of most systems. The displays may be driven at frame rates up to 75 Hz.

The EL512.256–H3 displays require +5 V_{DC} and +11…+30 V_{DC} power input and four basic input signals to operate:

- Video Data or pixel information
- Video Clock, pixel clock, or dot clock
- Horizontal Sync
- Vertical Sync

2 TFEL technology

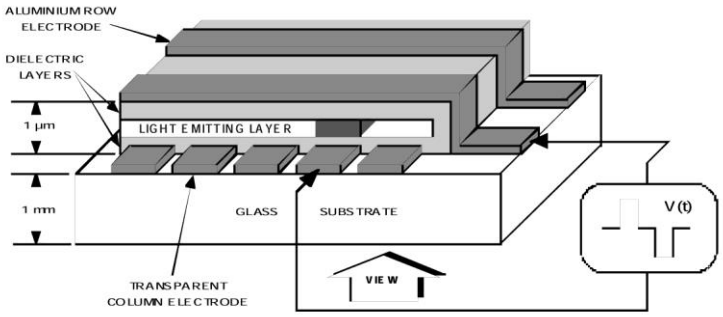


Figure 1. TFEL technology

A display consists of an electroluminescent glass panel and a mounted circuit board with control electronics. The TFEL glass panel is a solid-state device with a thin film luminescent layer sandwiched between transparent dielectric layers and a matrix of row and column electrodes. The row electrodes, in back, are aluminum; the column electrodes, in front, are transparent. The entire thin film device is deposited on a single glass substrate. The glass panel is mounted to an electronic circuit assembly board (ECA) with an elastic spacer. The ECA is connected to the TFEL glass panel with soldered lead frames. The result is a flat, compact, reliable and rugged display device.

In the EL512.256–H3 series displays, the 512 column electrodes and 256 row electrodes are arranged in an X-Y formation with the intersecting areas performing as pixels. Voltage is applied to both the correct row electrode and the correct column electrode to cause a lit pixel. Operating voltages required are provided by an integral DC/DC converter.

3 Electrical characteristics

3.1 Connector layout

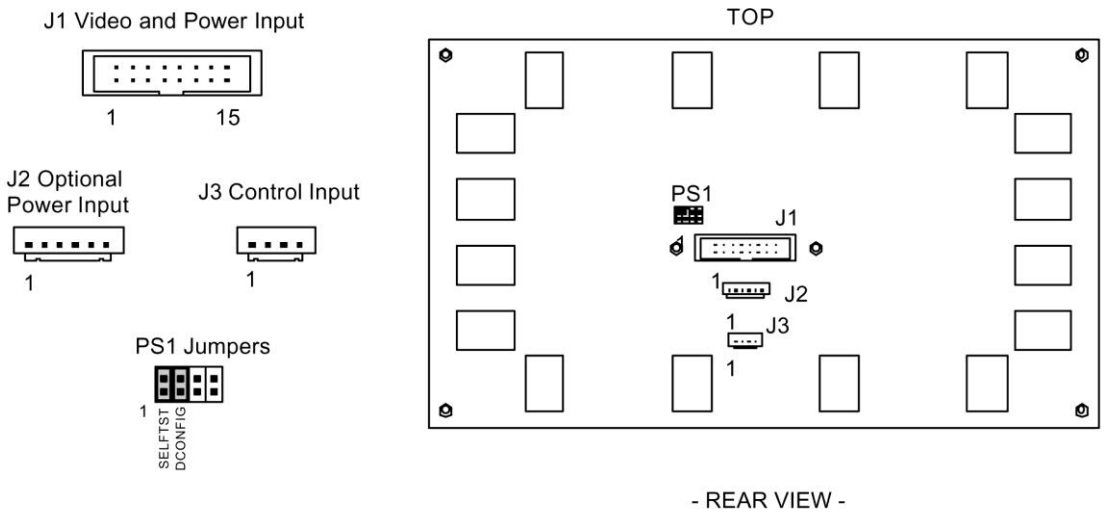


Figure 2. Input connectors and jumpers and their location

3.2 Input to the display

Table 1. Input to the display

Pins	Signal	Symbol	Description
J1(Data/power input connector)			
1, 2	Voltage	V_{cc2}	Supply voltage (+11 V …+30 V) converted to required internal high voltages (see J2).
3, 4	Voltage	V_{cc1}	Supply voltage (+5 V) for the logic (see J2).
5	Reserved		Reserved, do not connect.
6, 8, 10	Ground	GND	Signal return.
7	Two-bit data	TVID	Second data input for 2-bit parallel mode. The TVID input is for odd columns and the VID for even ones.
9	Vertical Sync	VS	The vertical sync signal VS controls the vertical position of the picture.
11	Horizontal Sync	HS	The horizontal sync signal HS controls the internal row counter and the horizontal position of the picture.

Pins	Signal	Symbol	Description
13	Video Clock	VCLK	The VCLK signal shifts data present on the VID and TVID lines into the display system. VCLK is active on the rising edge.
15	Video Data	VID	Signal that supplies the pixel information to the system.
12, 14, 16	Ground	GND	Signal return.
J2 (Optional power input connector)			
1	Voltage	V_{cc2}	Same as J1, Pins 1, 2 (not necessary to connect if power is supplied via J1).
2, 3	Ground	GND	Same as J1 Pins 6, 8, 10, 12, 14, 16 (not necessary to connect if power is supplied via J1).
4	Voltage	V_{cc1}	Same as J1 Pins 3, 4 (not necessary to connect if power is supplied via J1).
5	Low Power	_LOWPWR	The power consumption of the display is lowered to the LOWPWR values if the _LOWPWR is low, internally pulled high if left disconnected.
6	Enable	ENABLE	The operation of the display unit is disabled if the ENABLE input is low, internally pulled high if left disconnected.
J3 (Optional control input connector)			
1	Luminance Pot.1	LUMPOT1	Input for external luminance control (see page 8). Can be left disconnected.
2	Luminance Pot.2	LUMPOT2	Input for external luminance control. Can be left disconnected.
3, 4	Reserved		Reserved, do not connect.

3.3 Control basics

The TFEL panel has 512 transparent column electrodes crossing 256 row electrodes in an X-Y fashion. Light is emitted when an AC voltage is applied at a row-column intersection. The display operation is based on the symmetric, line-at-a-time data addressing scheme, which is synchronized by the external VS, HS, and VCLK input signals. The internal control signals and the high voltage pulses for the column and row drivers are generated internally by the control electronics. All control signal inputs are HCT-compatible with pull-up resistors.

3.4 Power input

The required supply voltages for the display are +5 V_{DC} (V_{cc1}) for the logic and +11 V… +30 V_{DC} input (V_{cc2}) for the integrated DC/DC converter. The high voltages needed for driving the display are generated by the DC/DC converter from the V_{cc2} input voltage. The input voltages can be connected either through J1 or J2.

3.5 Signal inputs

The connector J1 contains input for the video signals, the connector J2 contains two control inputs and the connector J3 contains input for external luminance control. The signals on J2 and J3 that are not used can be left disconnected.

3.6 Optional grounding

In order to improve the EMC properties of the display system, there is an option for the customer to tie together the signal ground of the display and the chassis of the user device. For this purpose, the four corner mounting nuts are each connected to the signal ground with 10 nF / 50 V capacitors. When using this option, please be aware of the possible risk of lowered isolation strength of the device and possible generation ground loops.

3.7 Connectors

Table 2. Connectors

J1	16-pin header	TE connectivity 2-1761603-6 or OUPIIN 3012-16G00SBA/OP6 or eq.
	Mating	TE Connectivity 1-1658526-1 or eq. or OUPIIN 1001 series.
J2	6-pin header	Hirose DF1–6P–2.5DSA or eq.
	Mating	Hirose DF1–6S–2.5 R 24 or eq.
	Protector	Hirose DF1–6A 1.33
J3	4-pin header	Hirose DF1–4P–2.5DSA or eq.
	Mating	Hirose DF1–4S–2.5 R 28 or eq.
	Protector	Hirose DF1–6A 1.33

Table 3. PS1

Position name	Function
1 SELFTST	Self-test function is selected if the SELFTEST jumper is OFF. In self-test, the input video data at VID and TVID inputs are displayed asynchronously without any other input signals.
2 DCONFIG	The two-bits-parallel mode is selected if this jumper is OFF (see page 8).
3 Reserved	Reserved, do not insert jumper.
4 Reserved	Reserved, do not insert jumper.

When shipped from the factory, the jumpers PS1/1 and 2 are set.

3.8 Input specifications

Table 4. Input specifications

Parameter	Symbol	Min.	Typ.	Max.	Absolute min./max.
Logic input HIGH		2 V			V_{cc1} + 0.5 V abs. max.
Logic input LOW				0.8 V	-0.5 V abs. min.
Logic supply voltage	V_{cc1}	4.75 V	5.0 V	5.25 V	6 V abs. max.
Logic supply current at 5 V	I_{cc1}	—	—	0.2 A	
Display Supply voltage	V_{cc2}	11 V	—	30 V	33 V abs. max.
Supply current at 12 V	I_{cc2}		0.5 A	0.9 A	
Supply current at 12 V (LOWPWR)	I_{cc2}		0.3 A	0.5 A	
Power consumption 5 V/12 V			6 W	12 W	
Power consumption 5 V/12 V (LOWPWR)			4 W	7 W	

Operating conditions: Frame rate 70 Hz, ambient temperature 25 °C.

NOTE: Absolute maximum ratings are those values beyond which damage to the device may occur. The minimum and maximum specifications in this Operations Manual should be met, without exception, to ensure the long-term reliability of the display. Beneq does not recommend operation of the display outside these specifications.

4 Display features

4.1 Video data input

Four input signals are needed for video input. VS signal marks the topmost row, HS envelopes the pixels in one row and VCLK indicates the valid pixel data. The visible pixels in a row are the last 512 pixels before the fall of the HS. The topmost row displayed is the first HS HIGH time ending after the rising edge of VS. If HS is running continuously, the rising edge of the VS can be simultaneous to the previous falling or rising edge of the HS.

See details on the timing as well as setup and hold timing on pages 9 and 10.

4.2 Two-bits-parallel data

To reduce the input data frequency, the video data can be input two bits per clock cycle. The two data inputs are organized so that the data for the odd columns, numbered from left to the right at the viewers side, is input at the TVID (J1/ pin 7) and the data for the even columns at VID (J1/ pin 15). The two-bits-parallel mode is selected by removing the jumper 2 of the pin strip header PS1.

4.3 Display enable

The display can be totally shut off for screen save or power reduction by a LOW sate in the ENABLE control input (J2/pin 6). When disabled, the display stops scanning and only the DC/DC converter remains functional, lowering the power consumption to below 2 W. In normal operation, the ENABLE input should be pulled HIGH or left disconnected (internal pull-up).

4.4 Brightness control

The brightness of the display can be adjusted (approximately between 40% and 100%) by an external 50 kΩ logarithmic potentiometer between the LUMPOT1 and LUMPOT 2 inputs (J3/pins 1 and 2). The control function is done by feeding a small DC current signal via the external potentiometer from LUMPOT1 (+5 V reference voltage) to LUMPOT2. If the two inputs are left disconnected, the brightness is at its maximum level.

4.5 Low power mode

The power consumption of the display can be reduced typically to 4 W by using the low power mode. This mode is selected when the _LOWPOW control input (J2/5) is pulled low. In normal operation, _LOWPOW should be pulled HIGH or left disconnected. In the low power mode, the contrast and average brightness of the display are slightly reduced.

4.6 Self-test

The operation of the display can be easily checked without any external signals by the self-test function.

- Remove the jumper 1 in the pin stripe PS1.
- Connect power to the display.

All pixels of the display will be lit except for the first half of the topmost row.

5 Installation and handling

The product should be mounted using the M3 insert nuts on the ECA. Beside the four corner nuts, it is recommended to use also the two center nuts in the mounting if the vibration or shock stress is severe.

Before touching the display, necessary precaution must be taken to prevent application of static charges on the display from the operator or tools.

The display is made of glass material and should be handled with proper care. Do not drop the display or allow hard objects to strike its surface.

NOTE: For trouble-free data transfer, a maximum cable length of 300 mm (12 in.) from data transmitter to display input connector is recommended. If longer cables up to 2 m (80 in.) length are needed, a serial resistor of approximately 47 Ω could be placed at each of the four signal line outputs of the transmitter in order to lower signal reflections.

Electrostatic Caution: The Beneq display uses CMOS and power MOS-FET devices. These components are electrostatic-sensitive. Unpack, assemble and examine this assembly in a static-controlled area only. When shipping, use packing materials designed for protection of electrostatic-sensitive components.

WARNING: The product generates potentially dangerous voltages capable of causing personal injury (high voltage pulses up to 195 V_{AC}). Do not touch the display electronics during operation!

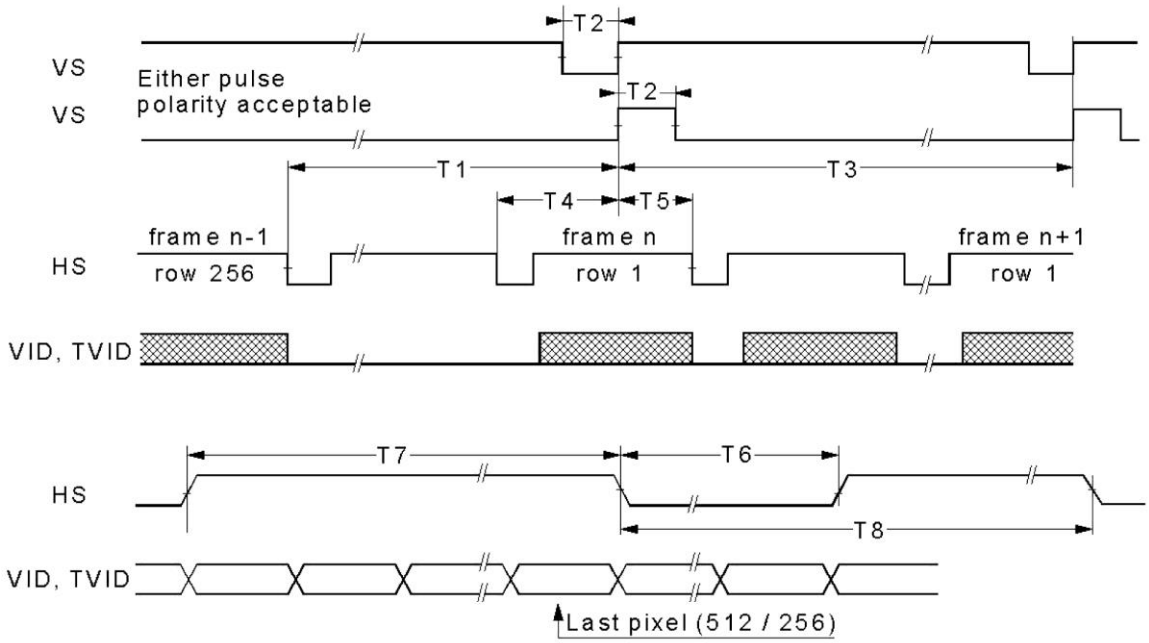


Figure 3. Video input timing

5.1 Video input timing

Table 5. Video input timing

Description	Min	typ	Max	Unit
T1 Vertical Front Porch [1]	100			µs
T2 VS HIGH/LOW time [2]	1			tVCLK
T3 Vertical Period	256 tHS + T1			
VS frequency		70	75	Hz
Description	**Min**	**Typ**	**Unit**	
T4 HS setup to VS	1		tVCLK	
T5 HS hold from VS	3		µs	
T6 HS Low Time [3]	4		tVCLK	
T7 HS High Time [4]	512	512	tVCLK	
T8 HS period (tHS)	50		µs	

Notes:

[1] This time is needed to display the last row and to change the frame.

[2] Only rising edge is used.

[3] Video Clock VCLK should be kept running.

[4] The values for two bit parallel mode are 256/256 tVCLK. The number of VCLK pulses during HS high time should be even.

5.2 Setup and hold timing

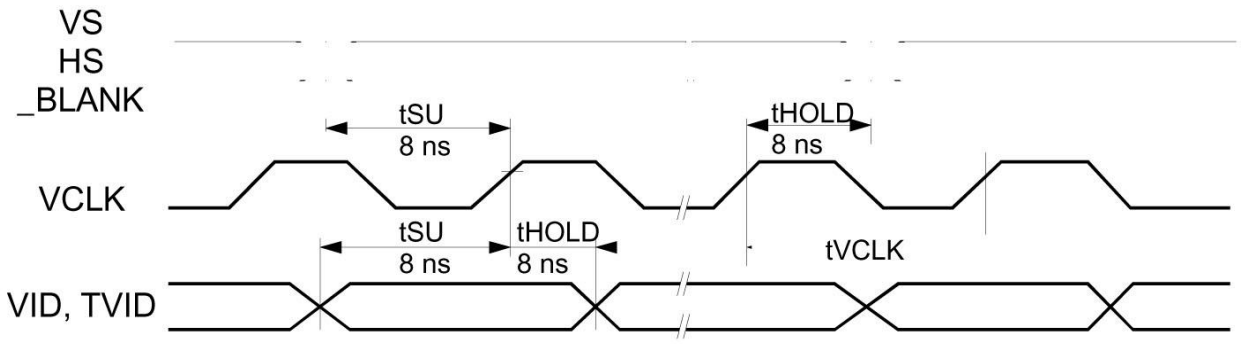


Figure 4. Setup and hold timing

Table 6. Setup and hold timing

Symbol	Description	Min	Max
tVCLK	VCLK period	33 ns	
	VCLK frequency		30 MHz

6 Operational specifications

6.1 Environmental

Table 7. Environmental characteristics

Temperature	
Operating	–25 °C …+65 °C
Non-operating	–40 °C …+75 °C
Operating survival	–40 °C …+65 °C (no permanent damage)
Test duration 24 h at temperature extremes (without condensation)	
Humidity	
Relative humidity	+40 °C, 93% RH, operating (IEC 60068-2-78)
Damp heat	+25 °C …+55 °C, 95% RH, non-operating (IEC 60068-2-30)
Altitude	
Operating	15,000 m (50,000 ft.) above sea level
Vibration	
	20…500 Hz ASD level 0.05 g^2/Hz Random vibration wide band IEC 60068-2-64, Test Fdb
Shock	
Magnitude Duration Number of shocks	100 G 4 ms (half sine wave) 18 (3 on each of the 6 surfaces) IEC 60068-2-27, test Ea

6.2 Reliability

MTBF > 30,000 h @ 25 °C

6.3 Safety

The display will not inhibit the end product from obtaining the following specification: UL544.

6.4 Optical

Determined at 70 Hz frame rate at room temperature.

6.4.1 Display color

Wide band amber (Zn:Mn)

Table 8. Optical characteristics

Areal luminance		
On Luminance (typ)	65 cd/m^2 (19 fL)	
On Luminance (min.)	45 cd/m^2 (13 fL)	
Measured at the center and the four corners of the screen.		
Luminance non-uniformity		
Maximum	35%	= (1– min. luminance/max luminance) x 100. Maximum difference between any two of five points (center and four corners)
Luminance variation (time)		
Maximum	20%	10,000 h
Luminance variation (temperature)		
Typical	10%	over –25 °C …+65 °C range
Maximum	15%	
Viewing angle		
Minimum	160°	

6.4.2 Optional filter

For the best overall optical performance of the display, a neutral, gray, circular polarizing filter with anti-reflective coating or etch is the usual choice. This filter will make the reflective electrodes of the display darker and improve the contrast ratio. The anti-reflective coating on the filter should face the user.

7 Mechanical characteristics

7.1 Display external dimensions

Figure 6 shows the mechanical dimensions of a standard EL512.256–H3 series display unit. The display can also be delivered with an optional FRA aluminum frame or an FRB steel frame (see Figure 5 and Figure 6). Using FRB frames makes the display mounting compatible with MD512.256 displays. See Ordering Information on page 19.

Table 9. Display external dimensions

Height	136 mm	5.35 in.
Width	233 mm	9.17 in.
Depth	16.5 mm	0.65 in.
Weight	400 g	14 oz.

7.2 Display viewing area characteristics

Table 10. Display viewing area characteristics

Active area		
millimeters (inches)	height	97.5 (3.84)
	width	195.1 (7.68)
Pixel pitch		
millimeters (inches)	height	0.381 (0.015)
	width	0.381 (0.015)
Pixel size		
millimeters (inches)	height	0.25 (0.01)
	width	0.25 (0.01)
Pixel fill factor	43%	
Pixel matrix	512 horizontal by 256 vertical	

CAUTION: The ambient temperature of the display should not be allowed to exceed the environmental specifications (see Table 7). In most applications, an air gap of approximately 5 mm is recommended (see mechanical drawings). Some applications may require, however, a larger air gap or cooling of the display unit in the system. Note that this may slightly increase the total depth of the design.

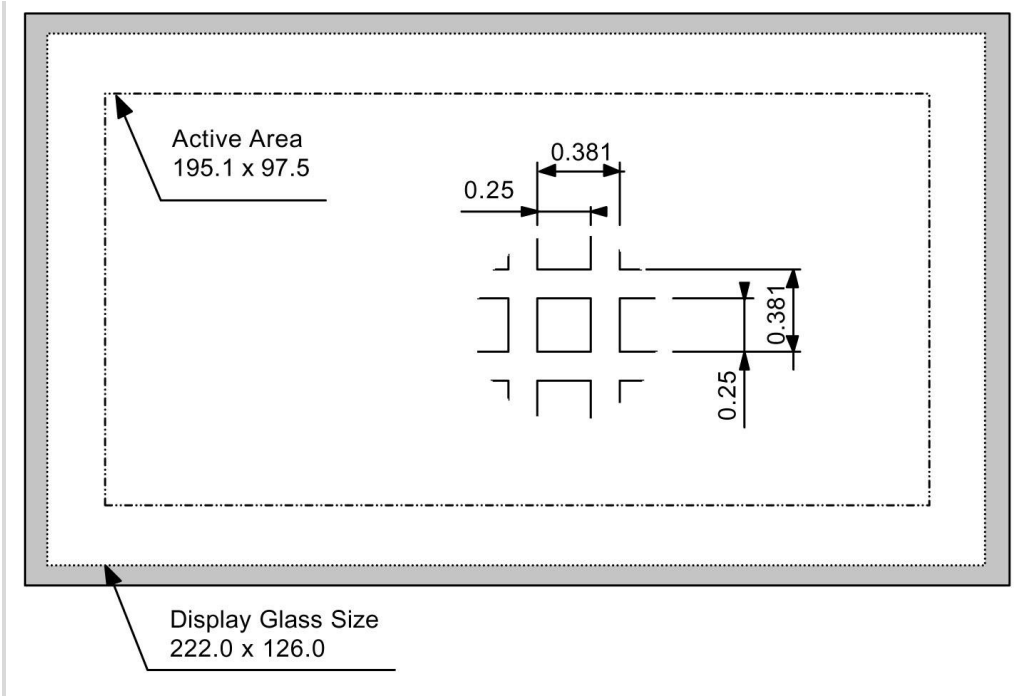


Figure 5. Viewing area characteristics

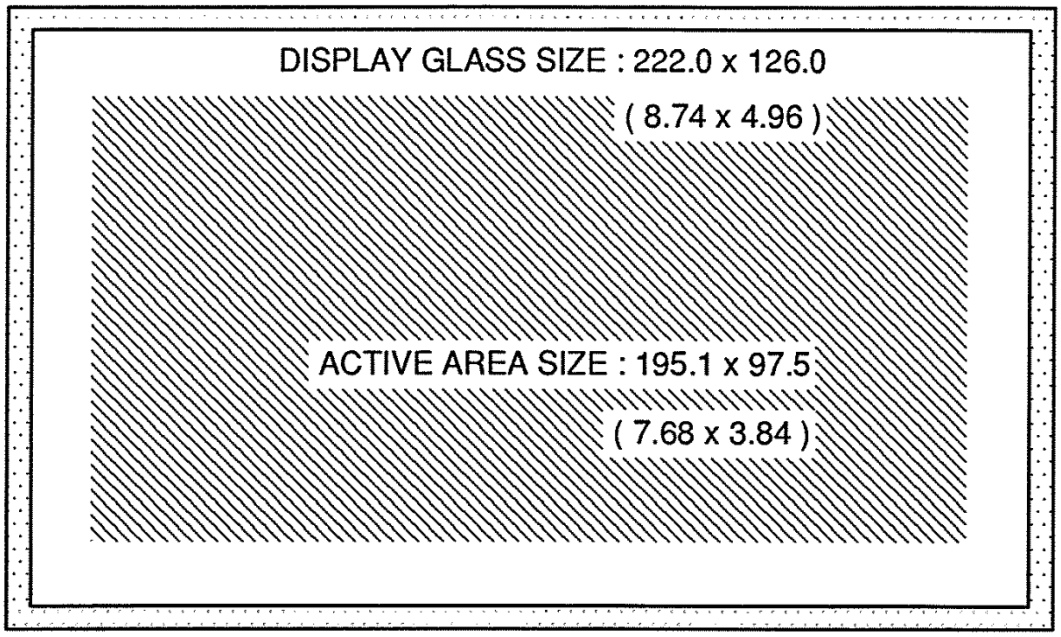
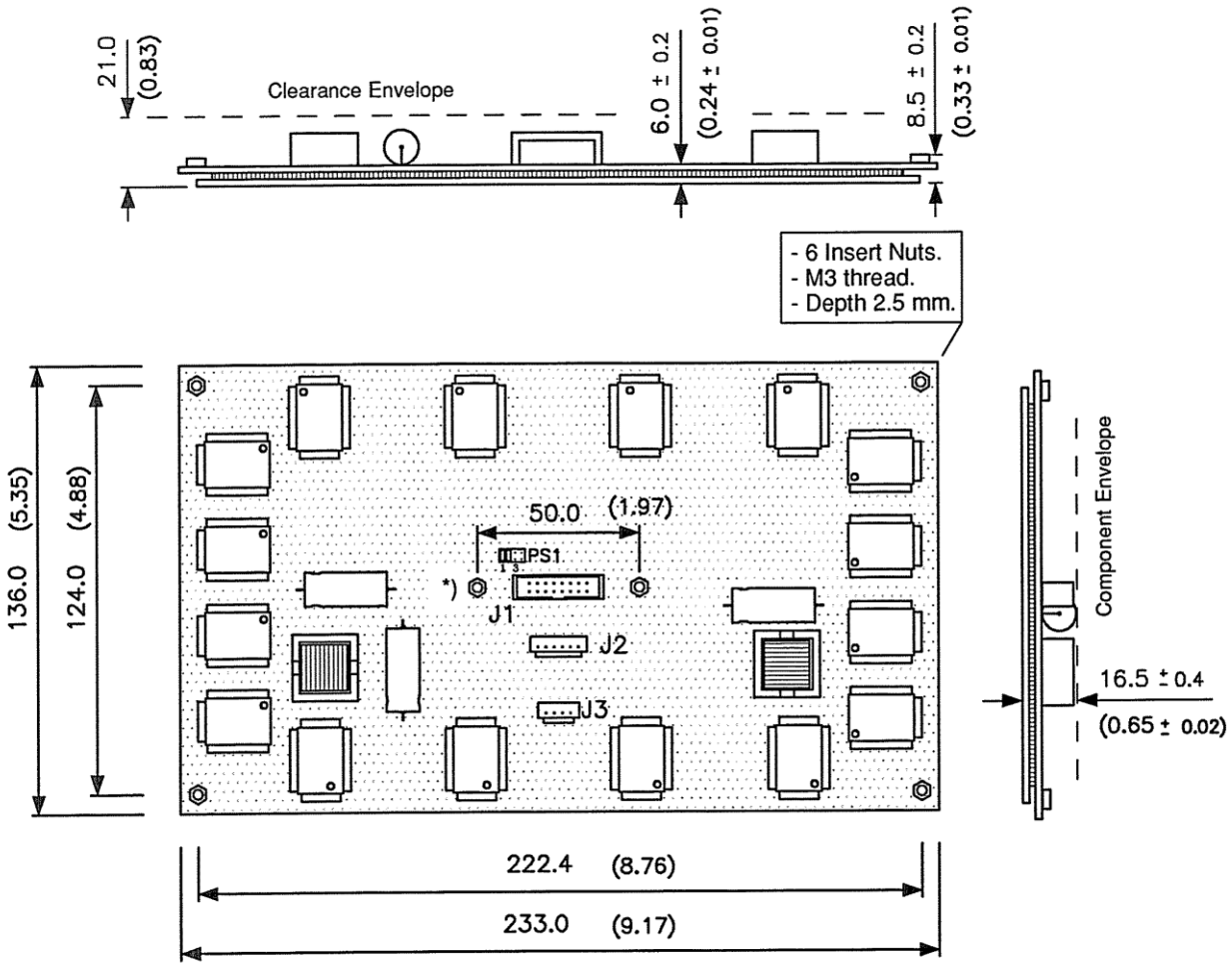


Figure 6. Front view without mounting frame (standard)



*) This Insert Nut is connected to System Ground.
Dimensions in mm (inches).

Figure 7. Back and side views (dimensions in mm)

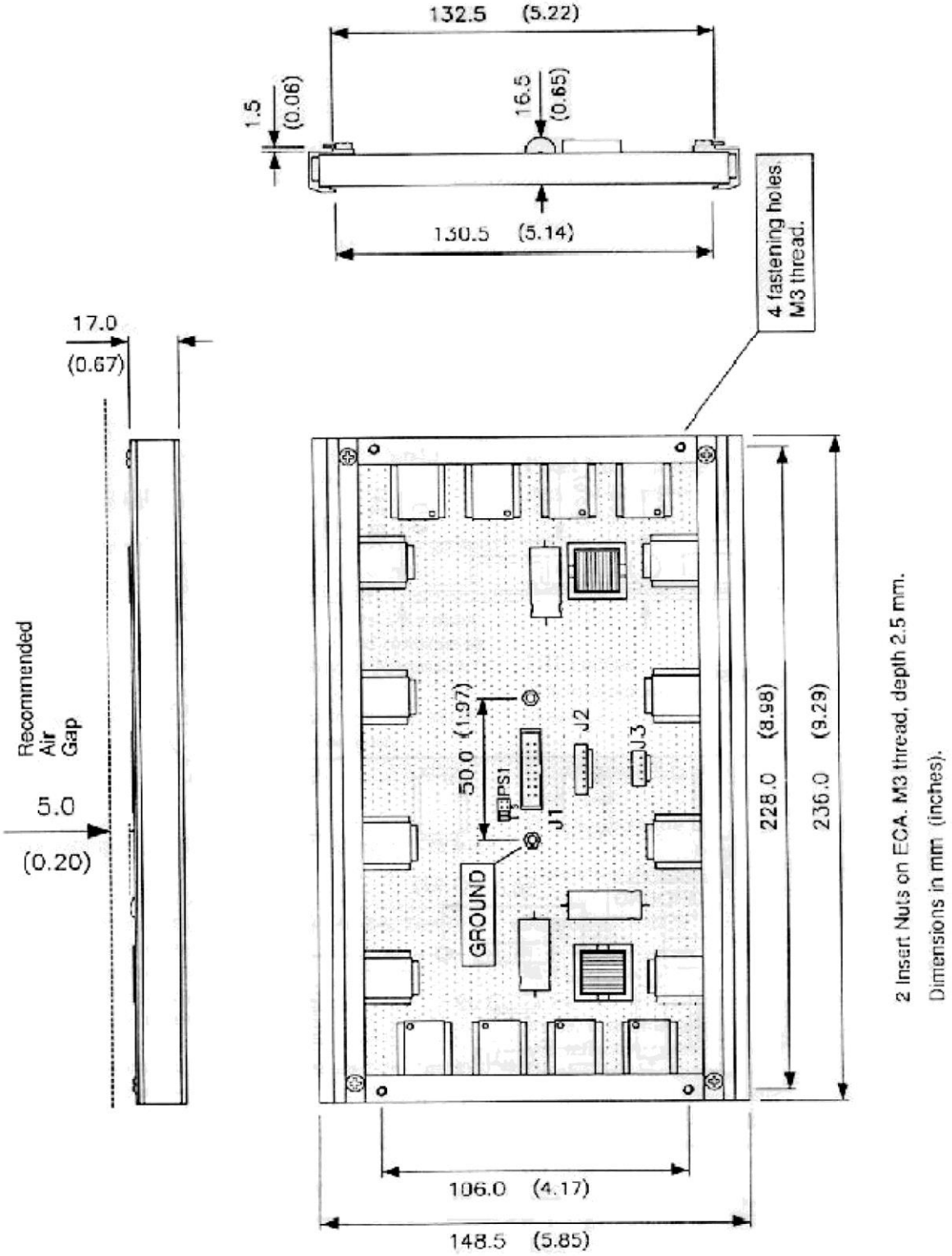


Figure 8. Back and side views with FRA aluminum mounting frame (dimensions in mm)

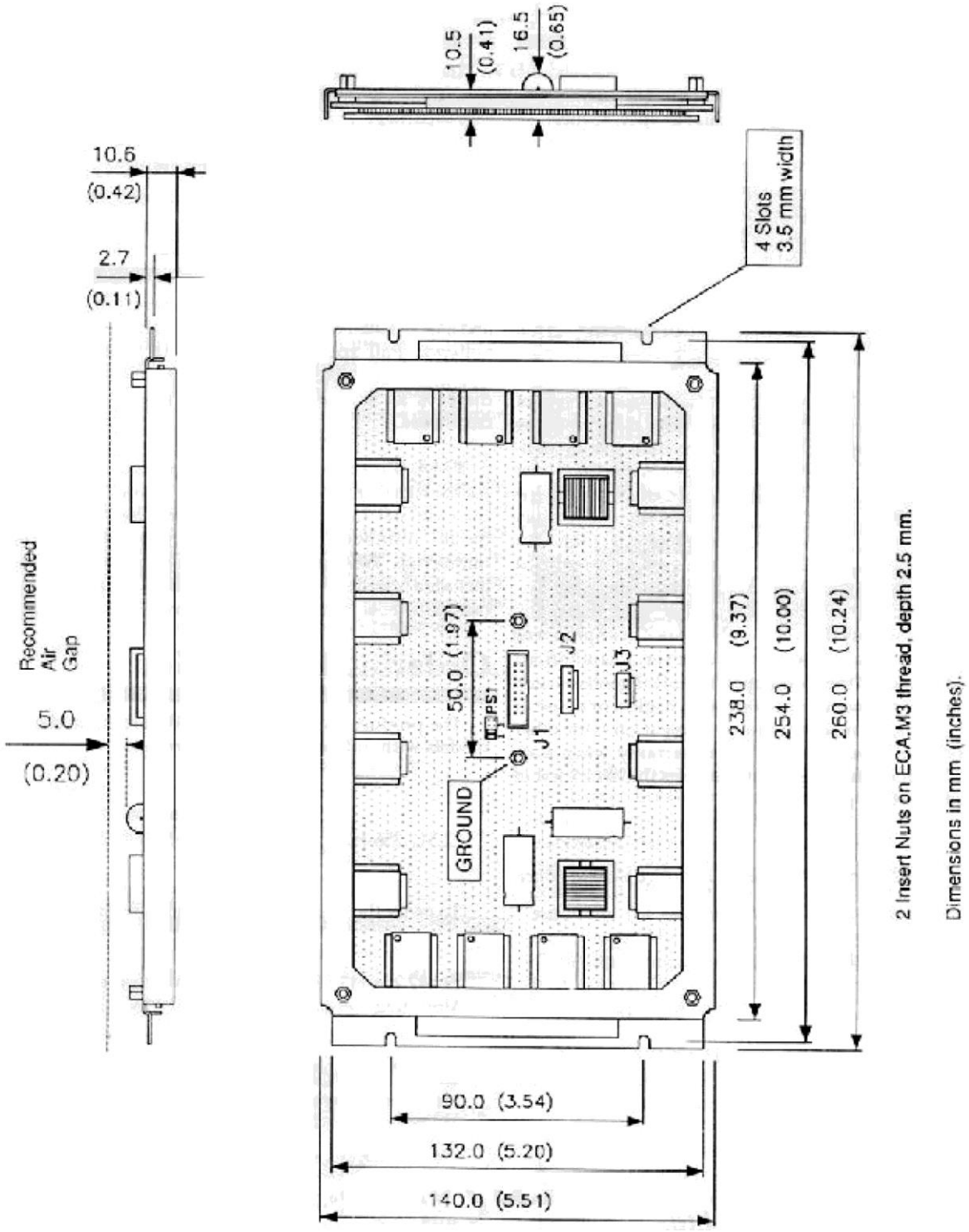


Figure 9. Back and side views with FRB steel mounting frame (dimensions in mm)

8 Description of warranty

Seller warrants that the Goods will conform to published specifications and be free from defects in material during warranty time from delivery. To the extent that goods incorporate third-party-owned software, seller shall pass on seller's licensor's warranty to buyer subject to the terms and conditions of seller's license.

Warranty repairs shall be warranted for the remainder of the original warranty period. Buyer shall report defect claims in writing to seller immediately upon discovery, and in any event, within the warranty period. Buyer must return goods to seller within 30 days of seller's receipt of a warranty claim notice and only after receiving seller's return goods authorization. Seller shall, at its sole option, repair or replace the goods.

If goods were repaired, altered or modified by persons other than seller, this warranty is void. Conditions resulting from normal wear and tear and buyer's failure to properly store, install, operate, handle or maintain the goods are not within this warranty. Repair or replacement of goods is seller's sole obligation and buyer's exclusive remedy for all claims of defects. If that remedy is adjudicated insufficient, Seller shall refund buyer's paid price for the goods and have no other liability to buyer.

All warranty repairs must be performed at seller's authorized service center using parts approved by seller. Buyer shall pay costs of sending goods to seller on a warranty claim and seller shall pay costs of returning goods to buyer. The turnaround time on repairs will usually be 30 working days or less. Seller accepts no added liability for additional days for repair or replacement.

If seller offers technical support relating to the goods, such support shall neither modify the warranty nor create an obligation of seller. Buyer is not relying on seller's skill or judgment to select goods for buyer's purposes. Seller's software, if included with goods, is sold as is, and this warranty is inapplicable to such software.

SELLER DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

9 Ordering information

Product	Part Number	Description
EL512.256–H3 FRA	996-5059-00LF	Aluminum mounting frame (mounting compatible with MD512.256–37C)
EL512.256–H3 FRB	996-5060-00LF	Steel mounting frame (mounting compatible with MD512.256–43/38/39 and EL6648MSS)

10 Support and service

Beneq Products is a Finnish company based in Espoo, Finland, with a world-wide sales distribution network. Full application engineering support and service are available to make the integration of Lumineq displays as simple and quick as possible for our customers.

RMA Procedure: For a Returned Material Authorization number, please contact Beneq Products Oy by email (rma.lumineq@beneq.com) with the model number(s), serial number(s) and brief description of the problem. When returning goods for repair, please include a brief description of the problem, and mark the outside of the shipping container with the RMA number.

11 RoHS III

Lumineq displays are RoHS3 (Restrictions of Hazardous Substances in Electronic/Electrical Equipment) compliant and meet the requirements defined under European Union Directive (2015/863), that restrict the use of various hazardous substances in electronic equipment.